

■ OVERVIEW

The SM5619 series is a range of quartz crystal oscillator ICs fabricated using NPC's original molybdenum-gate CMOS technology. Each IC consists of a low-current oscillator circuit and output buffer. With master slice, the output level can be selected between TTL and CMOS, and the output current between 16 mA and 4 mA. The IC also incorporates a high-precision, thin-film feedback resistor and oscillation capacitors having excellent frequency characteristics.

■ FEATURES

- Up to 30 MHz
- Fundamental wave
- Built-in feedback resistor in inverter amplifier
- Built-in loading capacitors CG and CD
- Output tristate function
- Low quartz current
- Chip form
- Input TTL compatible
- Operating voltage 4.5 to 5.5 V
- Low current consumption
- Chip form
- Molybdenum-gate® CMOS construction

■ PIN DESCRIPTION

Name	Function
XT	Oscillation input
XT	Oscillation output
INH	"L": output high impedance. Internal pull-up resistor.
V <sub>DD</sub>	Supply voltage
V <sub>SS</sub>	Ground
Q	Output (One of fo, fo/2, fo/4 and fo/8 is output according to internal wiring.)

■ SERIES LINEUP

Version	Output frequency	Output duty level	Output current (mA)
SM5619 N1	fo	CMOS	16
N3	fo/2	CMOS	16
N5	fo/4	CMOS	16
N7	fo/8	CMOS	16
H1	fo	CMOS	4
H3	fo/2	CMOS	4
H5	fo/4	CMOS	4
H7	fo/8	CMOS	4
K1	fo	TTL	16

BLOCK DIAGRAM

## ■ FUNCTIONAL DESCRIPTION

Control pin	Output pin
INH	Q
H (open)	One of fo, fo/2, fo/4 and fo/8
L	High impedance

fo: fundamental frequency

## ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

Item	Symbol	Rating		Unit
Supply voltage	V <sub>DD</sub>	-0.5 to +7.0		V
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5		V
Output voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5		V
Storage temperature	T <sub>STG</sub>	-65 to +150		°C
Output current	I <sub>OUT</sub>	H series	10	mA
		N series	25	
		K1 servion		

## ■ RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0V)

Item	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V <sub>DD</sub>	4.5	5.0	5.5	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub>		V <sub>DD</sub>	V
Operating temperature	T <sub>OPR</sub>	-20		+80	°C

## ELECTRICAL CHARACTERISTICS

1. N series, K1 version ( $V_{DD} = 5 \pm 0.5$  V,  $V_{SS} = 0$  V and  $T_a = -20$  to  $+80^\circ\text{C}$  unless otherwise specified)

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT	
				MIN	TYP	MAX		
H-level output voltage	$V_{OH}$	Q pin,	$V_{DD}=4.5\text{V}$ , $I_{OH}=16.0\text{mA}$	3.9	4.2		V	
L-level output voltage	$V_{OL}$	Fig. 1	$V_{DD}=4.5\text{V}$ , $I_{OL}=16.0\text{mA}$		0.3	0.4		
Output leak current	$I_z$	Q pin, Fig. 1, $\overline{\text{INH}}$ pin="L", $V_{DD}=5.5\text{V}$	$V_{OH}=V_{DD}$ $V_{OL}=V_{SS}$			10	$\mu\text{A}$	
H-level input voltage	$V_{IH}$	$\overline{\text{INH}}$ pin		2.0				
L-level input voltage	$V_{IL}$					0.8	V	
Current consumption	$I_{DD1}$	Load circuit 1, Fig. 2, $C_L=15\text{pF}$ , $\overline{\text{INH}}=\text{OPEN}$ , $f=30\text{MHz}$	SM5619N1	$C_L=15\text{pF}$		13	23	mA
				$C_L=50\text{pF}$		18	32	
			SM5619N3	$C_L=15\text{pF}$		9	16	
				$C_L=50\text{pF}$		12	21	
			SM5619N5	$C_L=15\text{pF}$		7	13	
				$C_L=50\text{pF}$		9	16	
			SM5619N7	$C_L=15\text{pF}$		6	11	
				$C_L=50\text{pF}$		7	13	
		SM5619K1	$C_L=15\text{pF}$		13	23		
Pull-up resistor	$R_{UP}$	$\overline{\text{INH}}$ pin, Fig. 3		50		250	$\text{k}\Omega$	
Feedback resistor	$R_f$	Fig. 4		90	100	110	$\text{k}\Omega$	
Inverter amplifier output resistor	$R_D$	Calculated from $R_f$		740	820	900	$\Omega$	
Internal capacitor	$C_G$			18.9	21	23.1	pF	
	$C_D$			18.9	21	23.1		

2. H series ( $V_{DD} = 5 \pm 0.5$  V,  $V_{SS} = 0$  V and  $T_a = -20$  to  $+80^\circ\text{C}$  unless otherwise specified)

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
H-level output voltage	$V_{OH}$	Q pin,	$V_{DD}=4.5\text{V}$ , $I_{OH}=4.0\text{mA}$	3.9	4.2		V
L-level output voltage	$V_{OL}$	Fig. 1	$V_{DD}=4.5\text{V}$ , $I_{OL}=4.0\text{mA}$		0.3	0.5	
Output leak current	$I_z$	Q pin, Fig. 1, $\overline{\text{INH}}$ pin="L", $V_{DD}=5.5\text{V}$	$V_{OH}=V_{DD}$ $V_{OL}=V_{SS}$			10	$\mu\text{A}$
H-level input voltage	$V_{IH}$	$\overline{\text{INH}}$ pin		2.0			
L-level input voltage	$V_{IL}$					0.8	V
Current consumption	$I_{DD1}$	Load circuit 1, Fig. 2, $C_L=15\text{pF}$ , $\overline{\text{INH}}=\text{OPEN}$ , $f=30\text{MHz}$	SM5619H1		11	20	mA
			SM5619H3		8	14	
			SM5619H5		6	11	
			SM5619H7		5	9	
Pull-up resistor	$R_{UP}$	$\overline{\text{INH}}$ pin, Fig. 3		50		250	$\text{k}\Omega$
Feedback resistor	$R_f$	Fig. 4		90	100	110	$\text{k}\Omega$
Inverter amplifier output resistor	$R_D$	Calculated from $R_f$		740	820	900	$\Omega$
Internal capacitor	$C_G$			18.9	21	23.1	pF
	$C_D$			18.9	21	23.1	

## ■ SWITCHING CHARACTERISTICS

### 1. N series

( $V_{DD} = 5 \pm 0.5$  V,  $V_{SS} = 0$  V and  $T_a = -20$  to  $+80^\circ\text{C}$  unless otherwise specified)

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Output rise time	$T_r$	Load circuit 1, Fig. 2 0.1V <sub>DD</sub> to 0.9V <sub>DD</sub>	CL=15pF	2.0	4.0	ns
			CL=50pF	4.0	8.0	
Output fall time	$T_f$	Load circuit 1, Fig. 2 0.9V <sub>DD</sub> to 0.1V <sub>DD</sub>	CL=15pF	2.0	4.0	ns
			CL=50pF	4.0	8.0	
Output duty cycle	DUTY	Load circuit 1, Fig. 2, V <sub>DD</sub> =5.0V, T <sub>a</sub> =25°C, C <sub>L</sub> ≤50pF	45		55	%
Output disable delay time	T <sub>PLZ</sub>	Fig. 2, V <sub>DD</sub> =5.0V,			100	ns
Output enable delay time	T <sub>PZL</sub>	T <sub>a</sub> =25°C, Load C <sub>L</sub> ≤50pF			100	
Maximum operating frequency	f <sub>MAX</sub>	Load circuit 1, Fig. 2, C <sub>L</sub> =50pF, Checked with lot monitor	30			MHz

### 2. H series

( $V_{DD} = 5 \pm 0.5$  V,  $V_{SS} = 0$  V and  $T_a = -20$  to  $+80^\circ\text{C}$  unless otherwise specified)

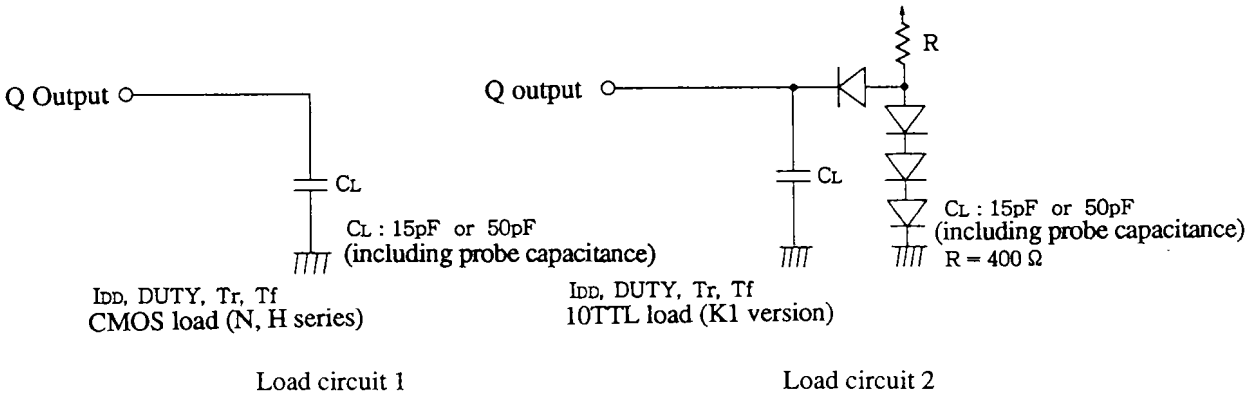
ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Output rise time	$T_r$	Load circuit 1, Fig. 2 0.1V <sub>DD</sub> to 0.9V <sub>DD</sub> , C <sub>L</sub> =15pF		5.0	10	ns
Output fall time	$T_f$	Load circuit 1, Fig. 2 0.9V <sub>DD</sub> to 0.1V <sub>DD</sub> , C <sub>L</sub> =15pF		5.0	10	ns
Output duty cycle	DUTY	Load circuit 1, Fig. 2, V <sub>DD</sub> =5.0V, T <sub>a</sub> =25°C, f=30MHz, C <sub>L</sub> =50pF	45		55	%
Output disable delay time	T <sub>PLZ</sub>	Fig. 2, V <sub>DD</sub> =5.0V, T <sub>a</sub> =25°C,			100	ns
Output enable delay time	T <sub>PZL</sub>	Load C <sub>L</sub> ≤15pF			100	
Maximum operating frequency	f <sub>MAX</sub>	Load circuit 1, Fig. 2, C <sub>L</sub> =15pF, Checked with lot monitor	30			MHz

### 3. K1 version

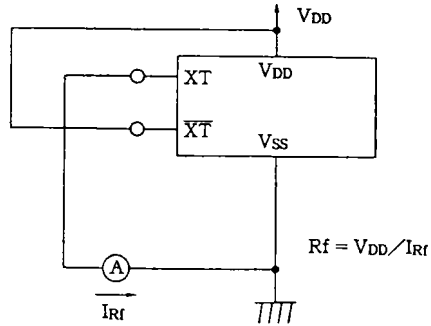
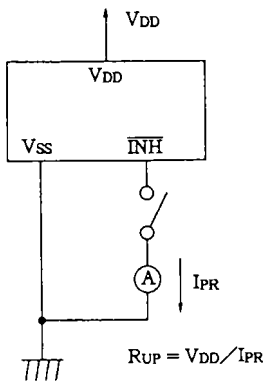
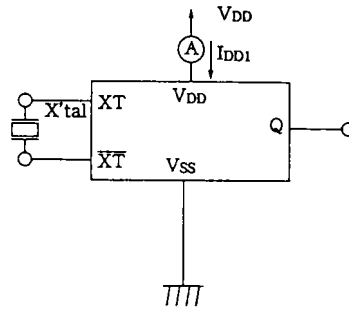
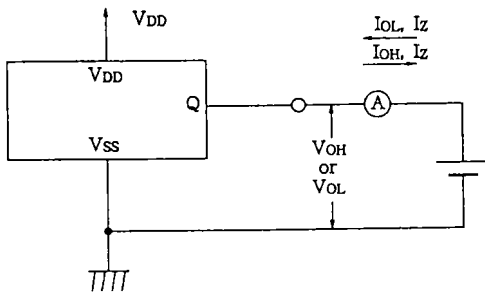
( $V_{DD} = 5 \pm 0.5$  V,  $V_{SS} = 0$  V and  $T_a = -20$  to  $+80^\circ\text{C}$  unless otherwise specified)

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Output rise time	$T_r$	Load circuit 2, Fig. 2 0.4V to 2.4V, C <sub>L</sub> =15pF		2.0	4.0	ns
Output fall time	$T_f$	Load circuit 2, Fig. 2 2.4V to 0.4V, C <sub>L</sub> =15pF		2.0	4.0	ns
Output duty cycle	DUTY	Load circuit 2, Fig. 2, V <sub>DD</sub> =5.0V, T <sub>a</sub> =25°C, f=30MHz, C <sub>L</sub> =15pF	45		55	%
Output disable delay time	T <sub>PLZ</sub>	Fig. 2, V <sub>DD</sub> =5.0V, T <sub>a</sub> =25°C,			100	ns
Output enable delay time	T <sub>PZL</sub>	Load C <sub>L</sub> ≤15pF			100	
Maximum operating frequency	f <sub>MAX</sub>	Load circuit 2, Fig. 2, C <sub>L</sub> =15pF, Checked with lot monitor	30			MHz

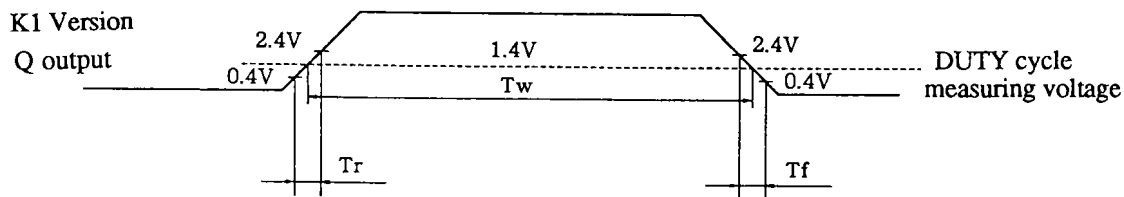
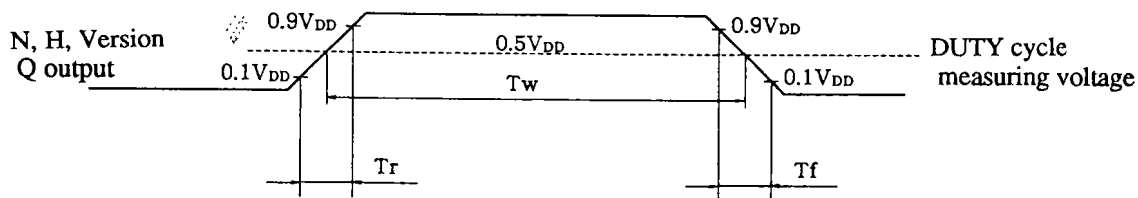
■ LOAD CIRCUIT



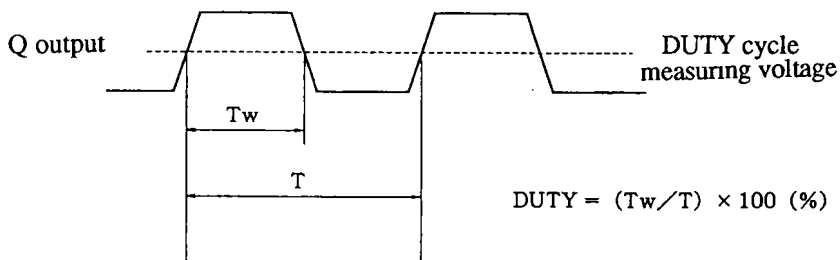
■ MEASURING CIRCUIT



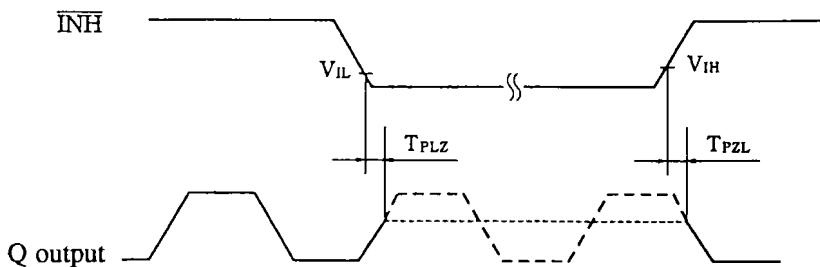
■ SWITCHING TIME WAVEFORM



■ OUTPUT DUTY CYCLE TIME

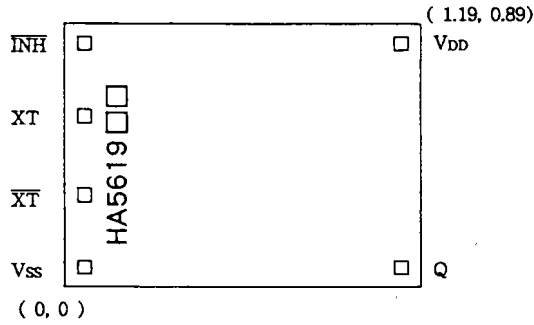


■ OUTPUT DISABLE DELAY TIME, OUTPUT ENABLE DELAY TIME V<sub>IL</sub>



Q output,  $\overline{\text{INH}}$  input waveform Tr = Tf 10 ns or less

■ PAD LAYOUT



Chip size: 1.19 × 0.89mm  
 Chip thickness: 400±30 μm

\* □□ version name

■ PAD COORDINATES (Unit: μm)

Pin name	X	Y
INH	183.5	707.5
XT	183.5	517.5
XT̄	183.5	327.5
Vss	183.5	137.5
Q	1042.5	141.5
VDD	1042.5	742.5