

**DISCONTINUED
PRODUCT**

OVERVIEW

The SM5004 Series crystal oscillator module ICs fabricated in NPC's Molybdenum-gate CMOS. They comprise low-voltage low-current consumption oscillator circuits

and output buffers. They incorporate built-in oscillation capacitance with superior frequency response to realize without any external components.

FEATURES

- Oscillation frequency up to 30MHz
- Fundamentally oscillation
- 4.5 to 5.5 V supply voltage
- Inverter amplifier feedback resistance built-in (R_f)
- Oscillation capacitances built-in (CG and CD)
- Output drive capability : 8 mA ($V_{DD}=4.5V$)
- Output frequency : f_0 , $f_0/2$, $f_0/4$, $f_0/8$
- Output duty level
CMOS, TTL, CMOS & TTL
- Input level : TTL
- 3 state function
- Chip form (CF5004××)
- 6 pin SOT (SM5004××H)

DEVICE LIST

Device	Output duty level	Output frequency	Output (standby)
SM5004A1H	CMOS	f_0	Hi-Z (Stop oscillation)
SM5004A3H	CMOS	$f_0/2$	Hi-Z (Stop oscillation)
SM5004A5H	CMOS, TTL	$f_0/4$	Hi-Z (Stop oscillation)
SM5004A7H	CMOS, TTL	$f_0/8$	Hi-Z (Stop oscillation)
SM5004B1H	TTL	f_0	Hi-Z (Stop oscillation)
SM5004B3H	TTL	$f_0/2$	Hi-Z (Stop oscillation)

Notes:

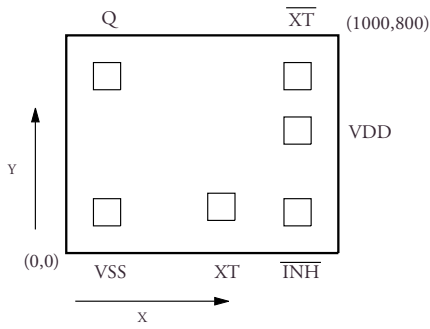
CF5004×× is Chip form.

SM5004××H is 6 pin SOT.

SM5004 Series
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PAD DIMENSIONS

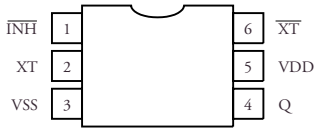
PAD COORDINATES



Name	Coordinates (μm)	
	X	Y
VSS	150	150
XT	570	170
$\overline{\text{INH}}$	850	150
VDD	850	450
$\overline{\text{XT}}$	850	650
Q	150	650

Chip size : 1.00x0.80 mm
Chip thickness : 250 ± 30 μm
Chip reverse side : VDD level

PIN CONFIGURATION (Top view)

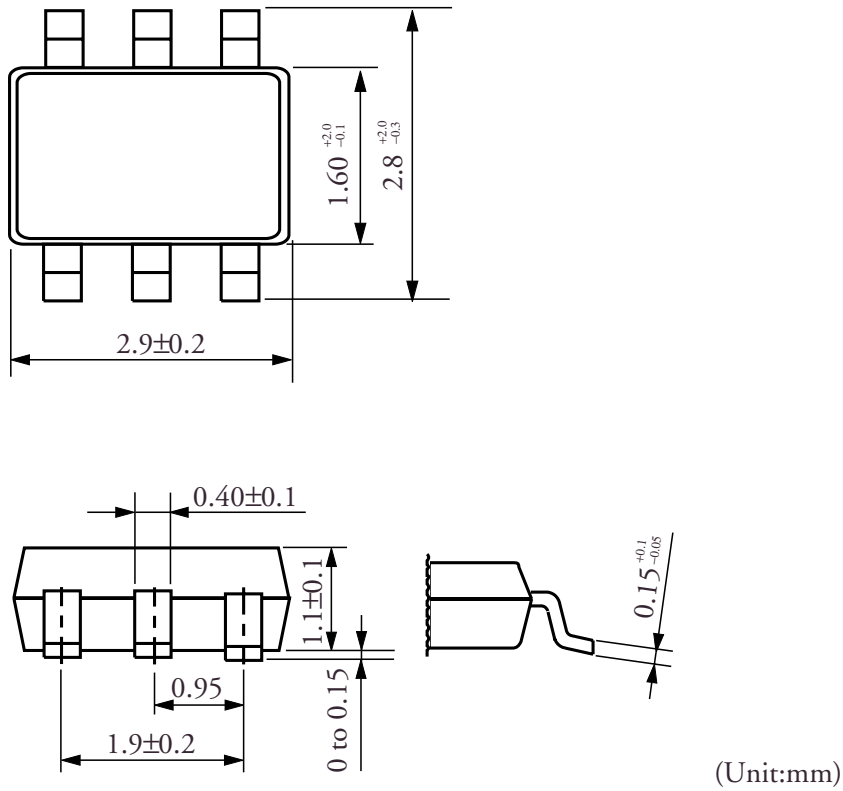


TERMINAL DESCRIPTIONS

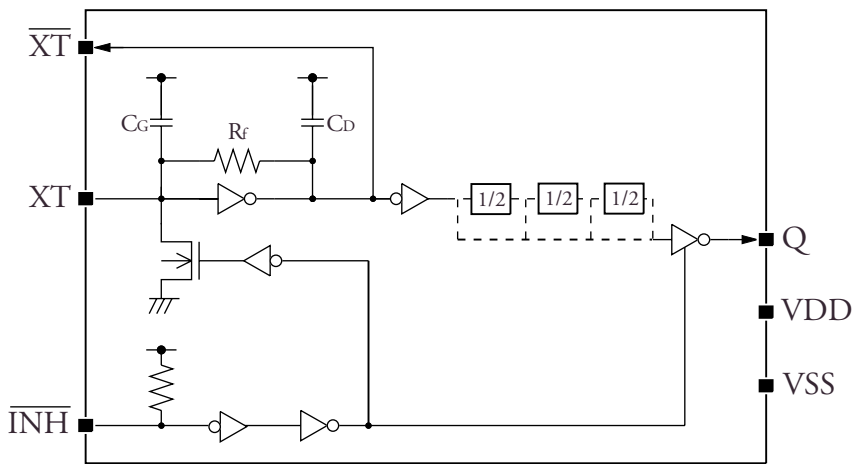
Name	Descriptions
XT	Oscillator input pin
$\overline{\text{XT}}$	Oscillator output pin
$\overline{\text{INH}}$	Output state control input pin (with built-in pull-up resistance)
VDD	Supply voltage
VSS	Ground
Q	Output pin

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PACKAGE DIMENSIONS (6 pin SOT)



BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

(V_{SS} = 0V unless otherwise noted)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V _{DD}		-0.5 to 7.0	V
Input voltage range	V _{IN}		-0.5 to V _{DD} + 0.5	V
Output voltage range	V _{OUT}		-0.5 to V _{DD} + 0.5	V
Storage temperature ranges	T _{STG}	Chip form	-65 to 150	°C
		6 pin SOT	-55 to 125	°C
Power dissipation	P _W	6 pin SOT	250	mW
Output current	I _{OUT}		13	mA
Soldering temperature	T _{SLD}	6 pin SOT	255	°C
Soldering time	t _{SLD}	6 pin SOT	10	sec

Recommended Operating Conditions

(V_{SS} = 0V unless otherwise noted)

Parameter	Symbol	Condition	Limit			Unit
			MIN	TYP	MAX	
Supply Voltage	V _{DD}		4.5		5.5	V
Input voltage	V _{IN}		V _{SS}		V _{DD}	V
Operating temperature	T _{OPR}		-20		+80	°C

Electrical Characteristics

(V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, T_a = -20 to 80°C, unless otherwise noted)

Parameter	Symbol	Condition	Limit			Unit	
			MIN	TYP	MAX		
HIGH-level output voltage	V _{OH}	Q pin, test circuit 1, V _{DD} = 4.5V, I _{OH} = 8mA	3.9	4.2		V	
LOW-level output voltage	V _{OL}	Q pin, test circuit 2, V _{DD} = 4.5V, I _{OL} = 8mA		0.3	0.4	V	
Output leakage current	I _Z	Q pin, test circuit 2, INH = Low, V _{DD} = 5.5V	V _{OH} = V _{DD}		10	μA	
			V _{OL} = V _{SS}		10	μA	
HIGH-level input voltage	V _{IH}	INH pin	2.0			V	
LOW-level input voltage	V _{IL}	INH pin			0.8	V	
Current consumption	I _{DD}	INH = OPEN, test circuit 3, C _L = 15pF, f = 30MHz	SM5004A×H load circuit 1		9	14	mA
			SM5004B×H load circuit 2		9	14	mA
Pull-up resistance	R _{UP}	INH pin, test circuit 4	25	100	250	kΩ	
AC feedback resistance	R _f	test circuit 5	100	200	400	kΩ	
Internal capacitance	C _G	Design value, determined by the internal wafer pattern.	17	20	23	pF	
	C _D		17	20	23	pF	

Switching Characteristics

Duty level CMOS

($V_{DD}= 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -20$ to $80^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Condition	Limit			Unit
			MIN	TYP	MAX	
Output rise time	t_r	Test circuit 6, load circuit 1, $C_L = 15pF$ $0.1V_{DD}$ to $0.9V_{DD}$		3.5	7	ns
Output fall time	t_f	Test circuit 6, load circuit 1, $C_L = 15pF$ $0.9V_{DD}$ to $0.1V_{DD}$		3.5	7	ns
Output duty cycle	DUTY	Test circuit 6, $T_a = 25^{\circ}C$, $V_{DD} = 5.0V$ load circuit 1, $C_L = 15pF$, $f = 30MHz$ (*1)	45		55	%
Output disable delay time	t_{PLZ}	Test circuit 6, $T_a = 25^{\circ}C$, $V_{DD} = 5.0V$ load circuit 1, $C_L = 15pF$			100	ns
Output enable delay time	t_{PZL}				100	ns

Duty level TTL

($V_{DD} = 4.5$ to $5.5V$, $V_{SS} = 0V$, $T_a = -20$ to $80^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Condition	Limit			Unit
			MIN	TYP	MAX	
Output rise time	t_r	Test circuit 6, load circuit 2, $C_L = 15pF$ $0.4V_{DD}$ to $2.4V_{DD}$		2.5	7	ns
Output fall time	t_f	Test circuit 6, load circuit 2, $C_L = 15pF$ $2.4V_{DD}$ to $0.4V_{DD}$		2.5	7	ns
Output duty cycle	DUTY	Test circuit 6, $T_a = 25^{\circ}C$, $V_{DD} = 5.0V$ load circuit 2, $C_L = 15pF$, $f = 30MHz$ (*1)	45		55	%
Output disable delay time	t_{PLZ}	Test circuit 6, $T_a = 25^{\circ}C$, $V_{DD} = 5.0V$ load circuit 2, $C_L = 15pF$			100	ns
Output enable delay time	t_{PZL}				100	ns

Note:

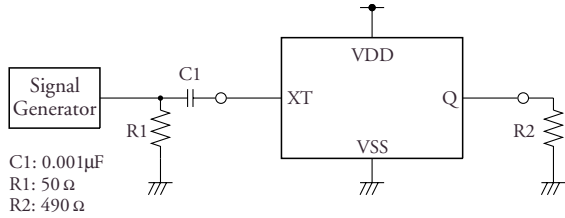
(*1) Determined by the lot monitor.

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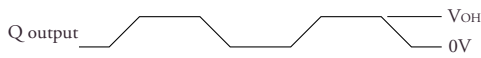
TEST CIRCUITS

Test Circuit 1

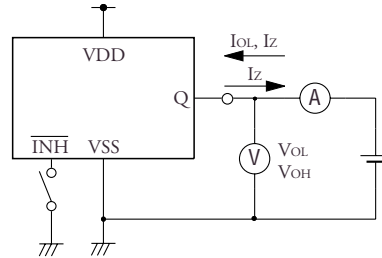
3.5 V_{P-P}, 10MHz sine wave input signal



C1: 0.001μF
R1: 50 Ω
R2: 490 Ω

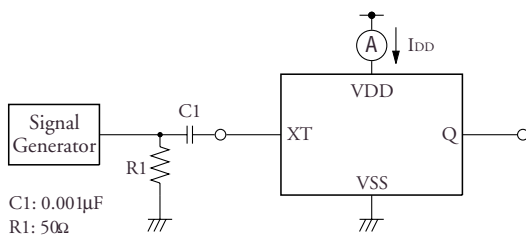


Test Circuit 2



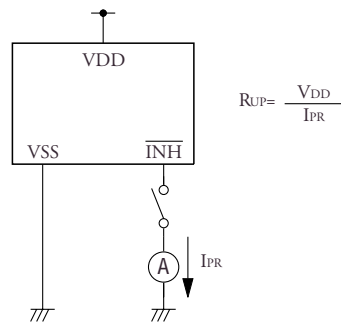
Test Circuit 3

3.5 V_{P-P}, 30MHz sine wave input signal

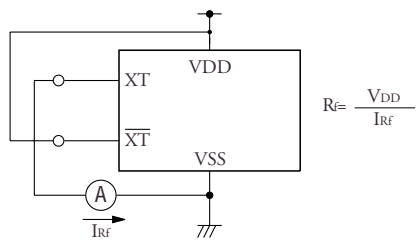


C1: 0.001μF
R1: 50Ω

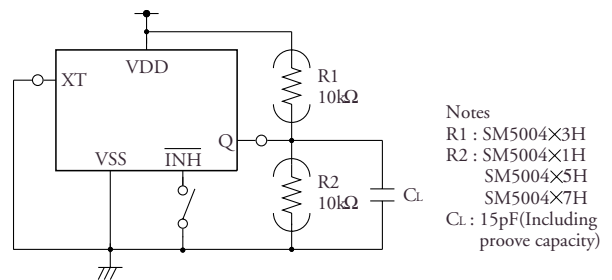
Test Circuit 4



Test Circuit 5

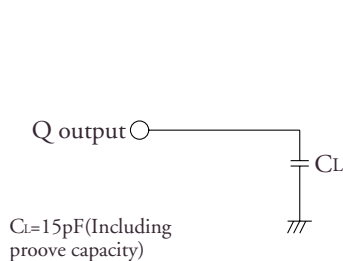


Test Circuit 6



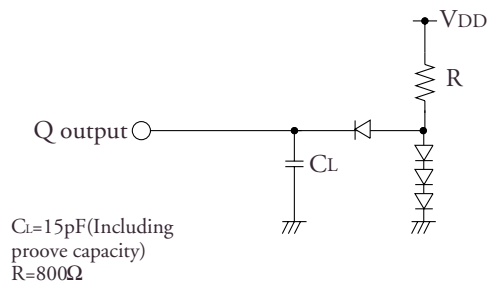
Notes
R1 : SM5004×3H
R2 : SM5004×1H
SM5004×5H
SM5004×7H
C_L : 15pF(Including proove capacity)

Load Circuit 1



C_L=15pF(Including proove capacity)

Load Circuit 2

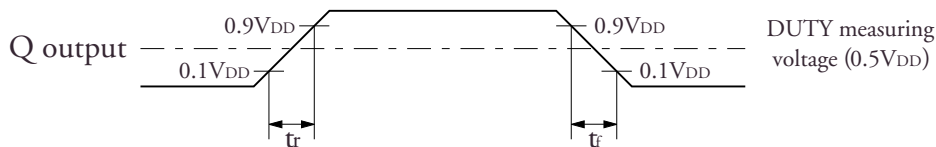


C_L=15pF(Including proove capacity)
R=800Ω

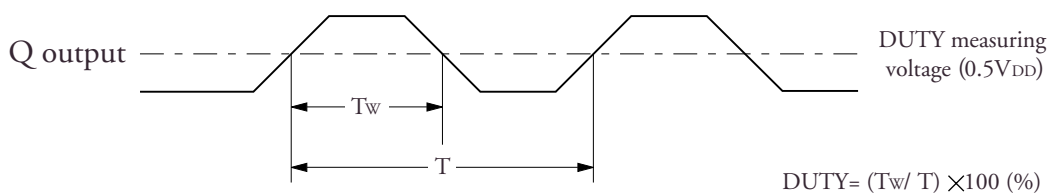
Switching Time Test Waveforms

Duty level CMOS

t_r, t_f DUTY

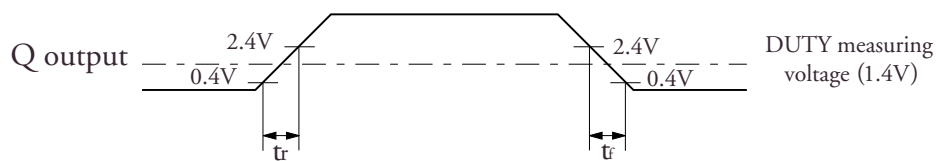


Output duty cycle time

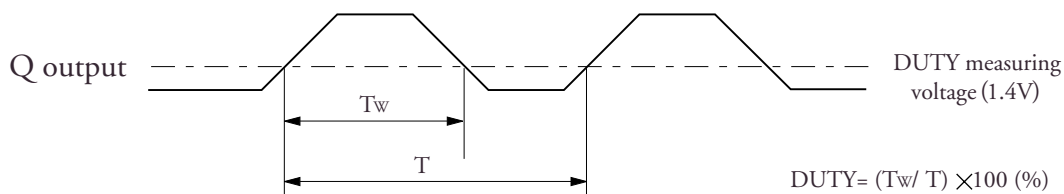


Duty level TTL

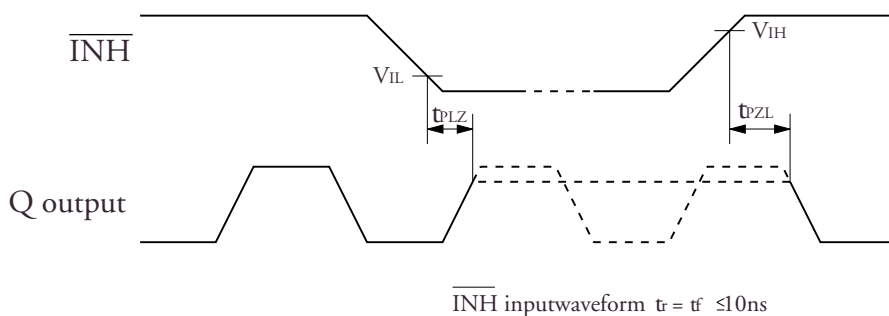
t_r, t_f DUTY



Output duty cycle time



Output Disable/Enable Delay Times



Note :

This waveform is provided by oscillating.

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